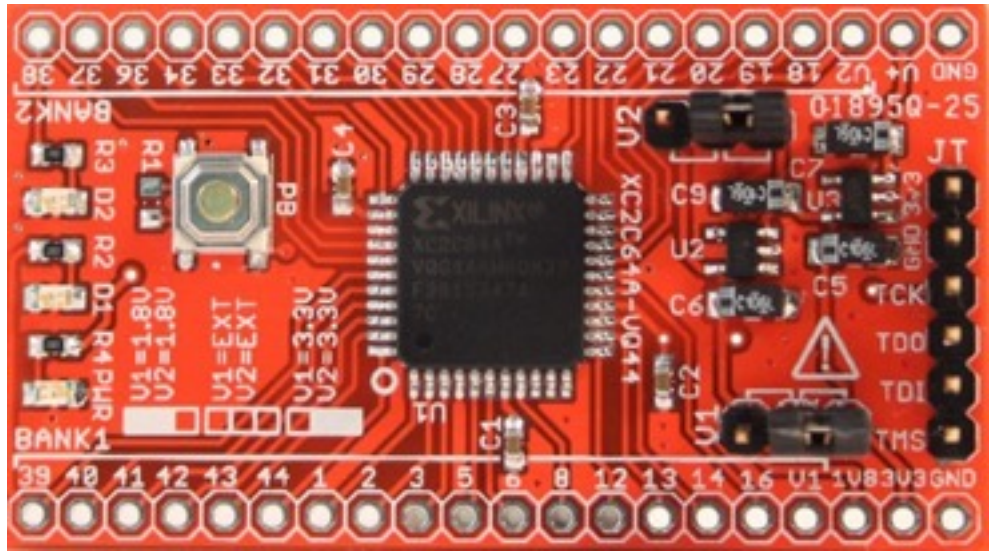
Complex Programmable Logic Device (CPLD)

Objectives

- Digital Design through Progammable Logic Devices in Verilog
- Frequency Divider (ex. tone generator for an audio device)



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1. Introduction

Boolean functions and Logic families

Boolean functions: Gates

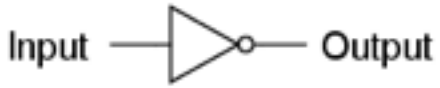
2-input OR gate

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

2-input AND gate

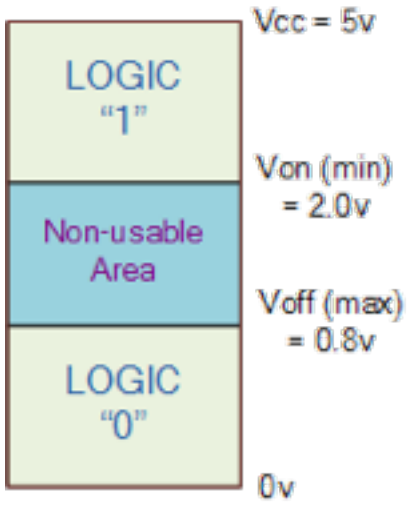
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Inverter, or NOT gate

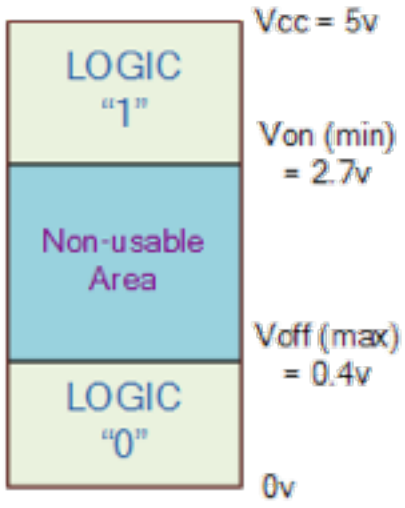


Logic Families

- TTL, CMOS, etc.
- Logic levels: MULTIMETER



LS - TTL Input Voltage levels



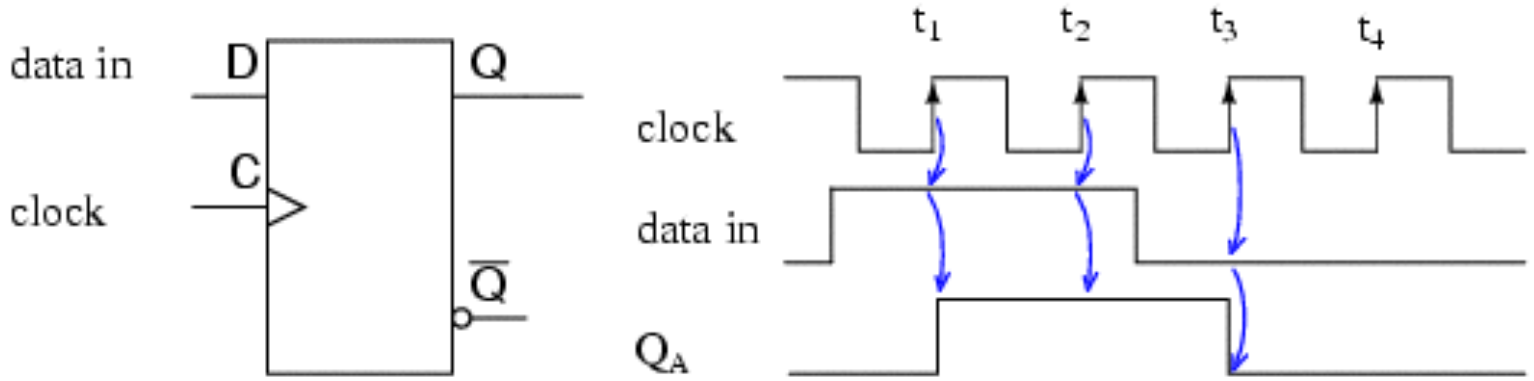
LS - TTL Output Voltage levels

2. Sequential Logic

Registers and Counters

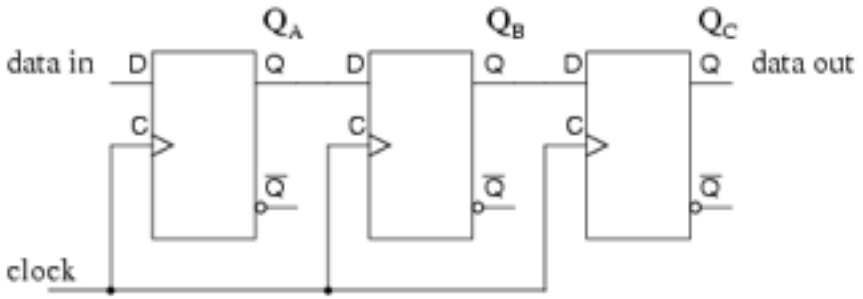
Registers

- Apart from the input, the output depends on the state (memory)
- Receiving data is not synchronized to the register clock



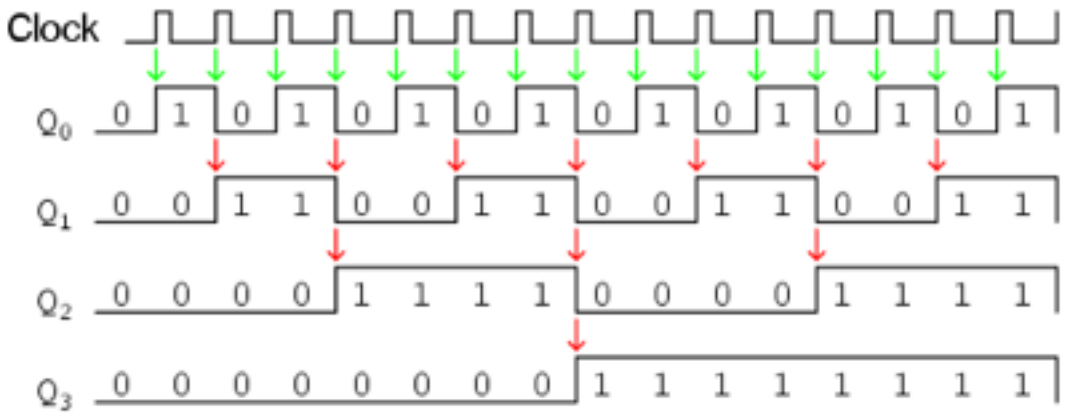
Data present at clock time is transfered from D to Q.

Shift register



Serial-in, serial-out shift register using type "D" storage elements

Binary counter



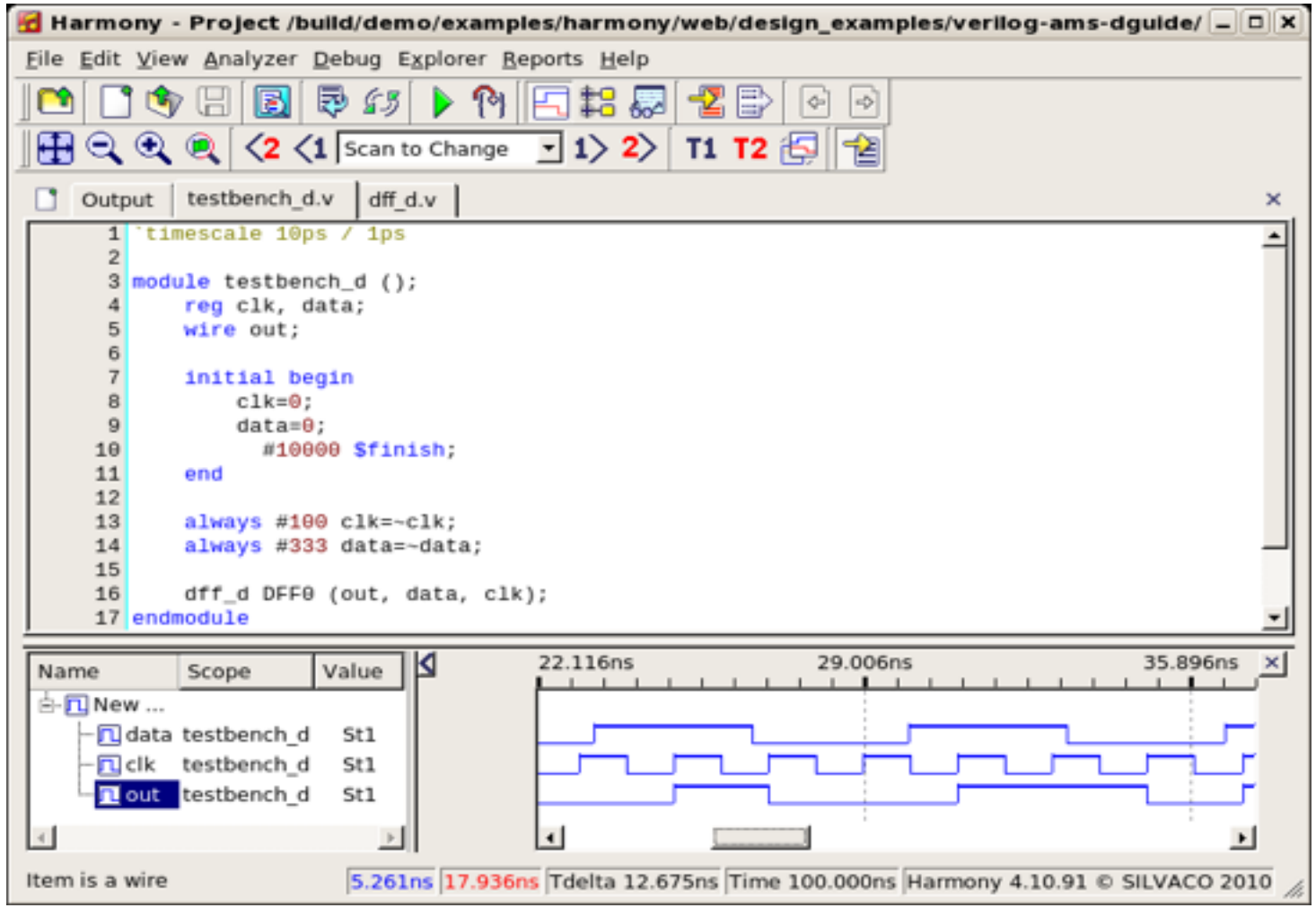
3. CPLD Features

CoolRunner II family and the Verilog language

CoolRunner II CPLD breakout board

- http://dangerousprototypes.com/docs/CoolRunner-II_CPLD_breakout_board
- CPLDs can give you the logic you need, with the pinout you want, while saving board space and board revisions.
- The platform has two separate banks of pins that can operate at different voltages (1V8 to 3V3) with internal pull-up resistors
- Disadvantages:
  - No banks at 5V (although the +V power supply)
  - ISE WebPack and Xilinx USB Cable (JTAG) is required

Verilog test-bench



Verilog designs

```
// Flip flop register
reg out;
always@(posedge clk)
begin
        out <= data;
end
```

```
// Binary counter
reg [3:0] counter;
always@(posedge clk)
begin
        counter <= counter + 1;
end
```

Questions

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